A 2.5V CMOS Switched-Capacitor Channel-Select Filter with Image Rejection and Automatic Gain Control

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Abstract **This paper presents a channel-select filter for 2.4GHz low-IF Bluetooth transceiver application. Besides of channel selection, image signal rejection, automatic gain control (AGC) and signal strength indication functions are all integrated. High frequency accuracy and large signal dynamic range is given as the switched-capacitor (SC) structure. Circuit techniques like multiple clock rate, filter capacitance scaling, and simplified op-amp structure are employed for power minimization. Measurement results indicate that the image rejection and the adjacent channel selectivity are better than 40dB and 60dB respectively. With a 0.25μm 1P5M CMOS technology the proposed filter dissipates 11.8mA from a single 2.5V supply voltage.**

I. Introduction

Channel selection is a delicate function in wireless transceiver design since it has to extract the obscure signal from large adjacent channels and other interferences. A low-IF architecture, as shown in Fig. 1, is proposed to alleviate these difficulties. At the last stage of frequency down conversion, the desired band is shifted to a relevant low frequency as half channel bandwidth away from DC. Therefore, low frequency offset voltage caused by circuitry mismatch which may also degrade the receiver sensitivity can be avoided. On the other hand, the adjacent channel known as the mirror signal will also be mixed down to the same low-IF frequency. Therefore, image rejection function associated with the channel selection is required.

Different from using high-Q bandpass filter in high-IF, one method to achieve image rejection is using complex signal processing in low-IF architecture. There are several approaches available in active complex filter design [1][2]. However, most of them are continuous-type. Tuning or trimming circuits are necessary to overcome the process variation for VLSI realization. The SC type, with its advantages of high frequency accuracy and large dynamic range, is very suitable for low IF application. Since the absolute capacitor values are independent of frequency, there is no need of large RC components which saves chip area. In addition, it takes an advantage of accurate gain adjusting by changing capacitor value. The AGC function can be incorporated with the filter architecture to reduce the signal dynamic range for the following demodulation. It can simultaneously be a received signal strength indicator (RSSI).

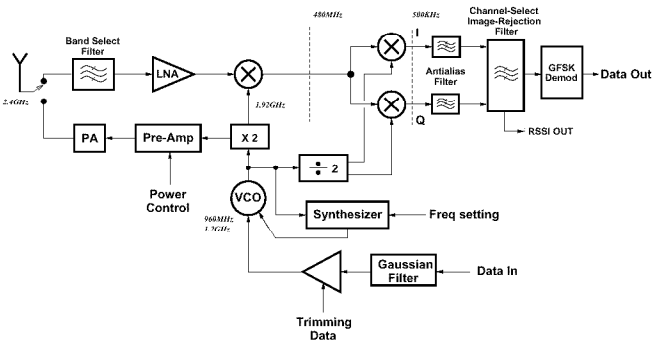

Figure 1: Transceiver block diagram.

II. Architecture and circuits design

A. Architecture design

Fig. 2 shows the architecture of the proposed active channel select filter. It includes three complex biquad filters, two first order highpass filter, one highpass biquad at signal path. A loop is closed for AGC function. MATLAB is used as the simulation platform to decide the type and order of the filter. The Butterworth-type is selected for its characteristic of small group delay. A bandpass transfer function composed of sixth-order lowpass and fourth-order highpass is used to reject the adjacent channel and DC offset voltage. The sixth-order lowpass filter is implemented with a cascade of three biquadratic sections. These arrangements will help circuit designs more flexible on optimizing overall dynamic range, power consumption, and noise reduction [3][4]. Among these biquads, two first order highpass filters are inserted to cancel the local DC offset. A second-order highpass filter serve as a buffer before output, and combines the quadrature signals at the same time.

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In this filter, the multi-rate strategy is employed to release the specifications of the preceding antialiasing filter [5]. Except for the first biquad that uses fast 26MHz sampling clock, all the others use 13MHz systematic clock.

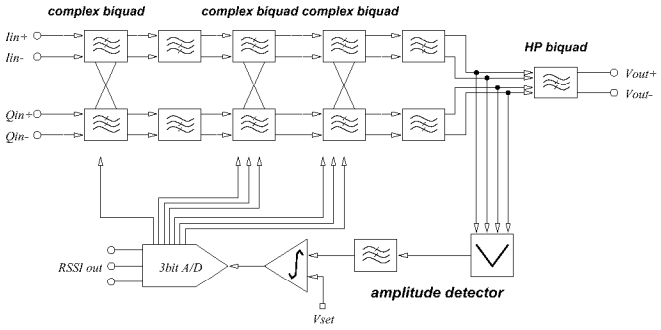

Figure 2: Block diagram of the novel image-rejection channel-select filter.

Instead of the traditional SC filter design methodology, directly implementing the filter with a z-domain transfer function. The concept of complex bandpass filter is frequency shifting from a real lowpass one. In z-domain, the operation is described as the following equation:

$$\begin{aligned} X_{bp}(z) &= X_{lp}(e^{-j\theta}z) \\ e^{-j\theta} &= cos\theta - jsin\theta \end{aligned} \quad (1)$$

where $\theta = 2f_c/f_s$, f_c is the shifting frequency as central frequency of complex bandpass filter and f_s is the sampling frequency. Fig. 3(a) and (b) show the architecture of the complex biquad filter quadrature paths I and Q respectively. In order to avoid the closed feedback loop, each biquad comprise an inverting integrator followed by a noninverting one. Since this circuit is directly derived from the z-domain transfer function, the stability can be guaranteed [5]. Moreover, utilizing SC type filter compresses efficiently the wanted signal called positive frequency and image signal call negative frequency crosstalk [1] due to the accurate matching of unit capacitance. Therefore, desirable image rejection can be achieved without auxiliary circuits.

The AGC function shown in Fig. 2 includes three complex biaquad filters as variable gain amplifiers, a rectifier and a lowpass filter as an amplitude detector, an integrator, and an A/D converter as an RSSI. To cover large dynamic range, the capacitor C1 and C1C of each biquad shown in Fig. 3 are binary capacitor arrays for gain control so that the gain is changed by 6dB per step. While the AGC loop is in steady state, output voltage is not constant instead of slowly periodic changing between two gain steps to achieve the

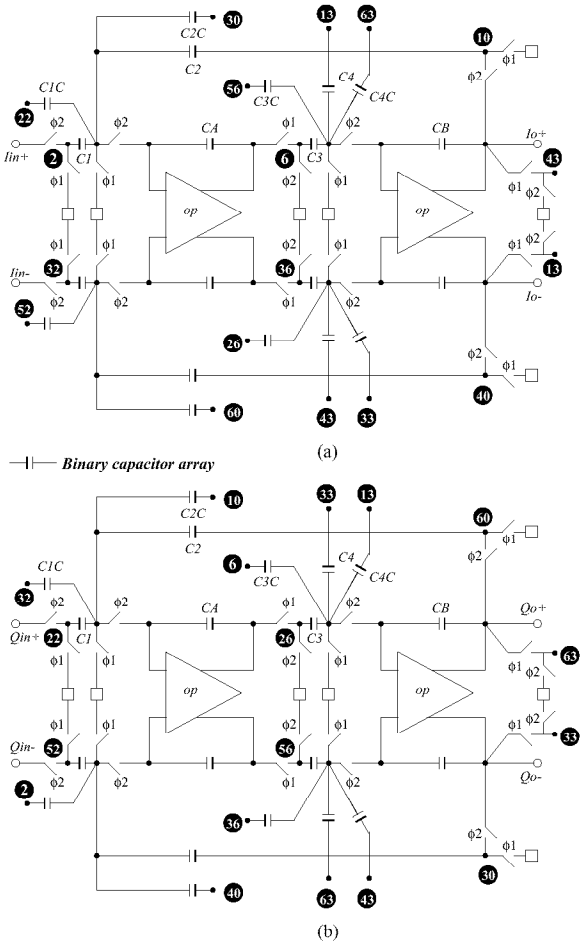

Figure 3: Block diagram of the complex biquad filter. (a) is the in-phase signal path and (b) is the quadrature-phase signal path.

output average value equal to setup voltage. Adjusting the pole location of lowpass filter and integrator unit-gain frequency can optimize the loop settling time. The analog output of integrator is digitized to 7 bits to control the capacitor array. At the same time, an encoder transfers the digitized signal to 3-bit RSSI signal output for overall transceiver power control.

B. Circuits design

In the first biquad stage of the filter, the capacitors are relevantly large to reduce the thermal noise (kT/C) of SC circuit. The capacitors in subsequent stages can be scaled down to optimize the power consumption [6]. According to the value of the capacitors, different switch device sizes are designed for better driving capability. The operational amplifier circuit used in the filter is a one-stage folded-cascode structure suitable for high speed application. Because of the capacitor scaling and multiple sampling rate strategies, the unit gain frequency of operational amplifiers in each filter stage are adjusted for power optimization.

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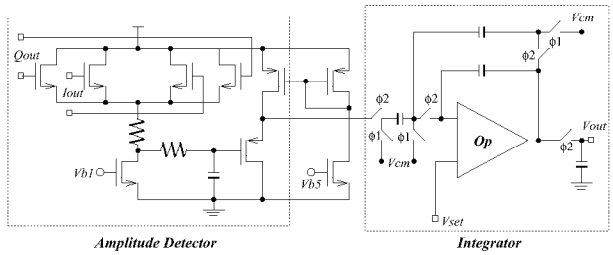
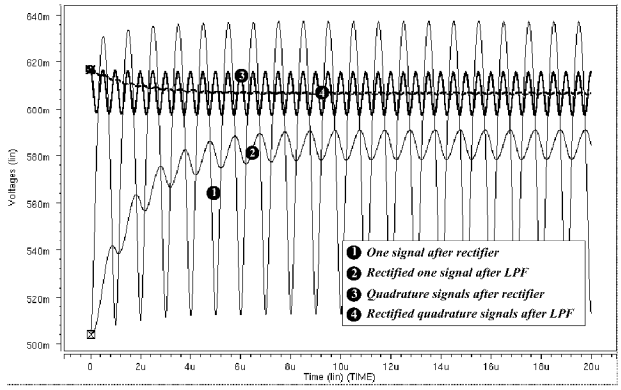
The amplitude detector, as shown in Fig. 4(a), comprises a rectifier circuit and a lowpass filter. Associated with the channel-select filter structure, the detector takes an advantage to extract the pair of quadrature signals simultaneously. Fig. 4(b) shows the simulation result of this amplitude detector with and without quadrature inputs. The ripple of the amplitude detector with quadratures inputs is much less while employing the same lowpass filter. A lowpass filter of relaxed specification can be used to improve the settling time of the AGC loop.



(a)



(b)

Figure 4: (a) Circuit diagram of the amplitude detector and integrator. (b) Simulation results of the amplitude detector with and without the quadrature signals.

The A/D converter shown in Fig. 5 is a flash architecture. It operates under a 13MHz sampling clock. The comparator used in the A/D can drive output with rail-to-rail [7]. Transistors Mr1 and Mr2 control the gain in tracking mode and improve the recovery at output nodes when the circuit goes from latching to tracking mode.

III. Measurement Results

Fig. 6 is the die photo of the proposed channel-select filter with image rejection and AGC functions. Using 0.25μm CMOS technology it occupies $1.7mm^2$. The frequency response of the overall filter is shown in Fig. 7. The image rejection at 500KHz is about 40dB. Fig. 8 shows outputs versus different inputs. The gain of the filter can vary from 14.4dB to 50.8dB while input

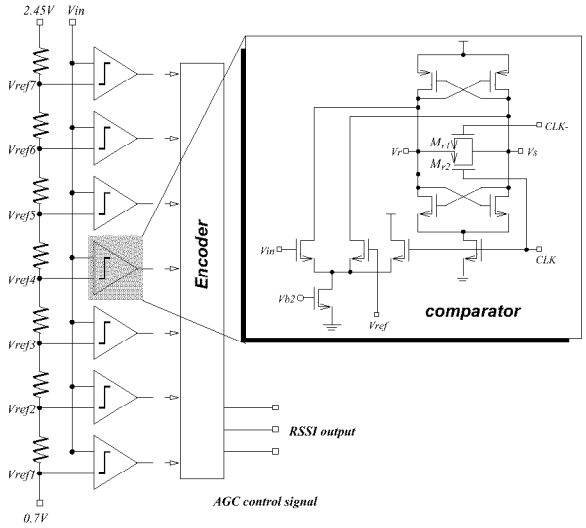


Figure 5: Circuit diagram of the A/D converter.

with 42.5dB dynamic range ($3mV_{pp}$-$400mV_{pp}$). The AGC loop can settle within 6μs.

The out-of-band third-order distortion is shown in Fig. 9. IIP3 is better than 20dBV. At each I/Q path the input referred voltage noise is $57nV/\sqrt{Hz}$. Table 1 is the performance summary of the overall circuitry.

Technology	0.25μm 1P5M MIM CMOS
Central Frequency f_c	500KHz
Bandwidth	900KHz w/ AGC
	810KHz w/o AGC
Sampling Rate f_s	26MHz,13MHz
Gain	14.4-50.8dB
Stopband attenuation	$> 60dB$
Image rejection	40dB@500KHz
IIP3	20dBV
Supply Voltage	2.5-V
Input referred noise	$57nV/\sqrt{Hz}$
Power Consumption	0.56mA/pole (filter core circuits)
	1.8mA (AGC feedback circuits)

Table 1: Performance summary of the proposed image-rejection channel-select filter.

IV. Conclusions

A proposed channel-select filter with image rejection and automatic gain control for the 2.4GHz Bluetooth receiver application is presented in this paper. It uses switched-capacitor type to achieve high frequency accuracy and dynamic range of signal. Applying quadrature signals to the amplitude detector, the AGC is with

fast settling behavior by 6μs. Multiple function are integrated in the filter while little area and power overhead are incorporated. This filter architecture with good channel selectivity while low power consumption is suitable for low-IF wireless communication system.

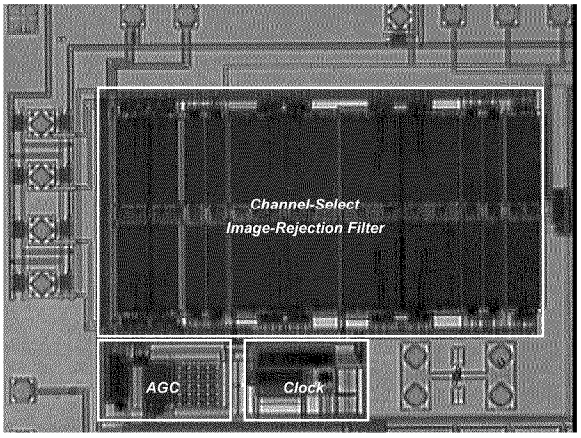


Figure 6: Die photo of the image-rejection channel-select filter.

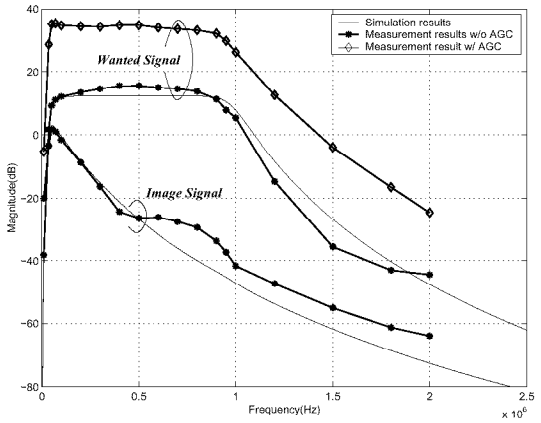


Figure 7: Frequency response of wanted signal and image signal.

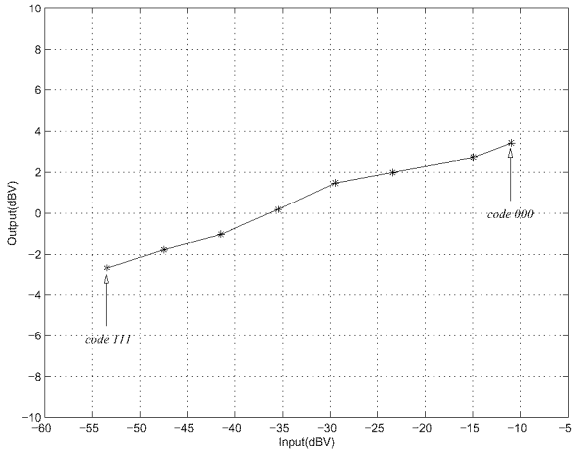


Figure 8: Output levels while different input magnitudes.

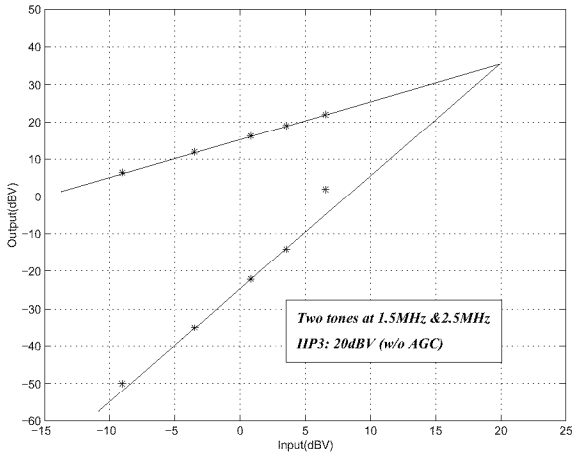


Figure 9: IIP3 measurement result while two tone at 1.5 and 2.5MHz.

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